## **Press Release**



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## EtherCAT ASIC available

The test phase of the Beckhoff ET1200 EtherCAT ASIC has been finished successfully, the chip – also known as "the small ASIC" – is now available.

In its QFN48 housing (7x7 mm) the chip is very compact. 16 digital I/O interfaces and the distributed clock feature for high precision synchronization are on board, a 10 Mbit serial interface allows one to access the I kByte internal DPRAM locally with process and parameter data. Two EtherCAT ports are available, out of which one can be configured as MII for connecting a standard PHY. The other port is used for LVDS, which makes the ET1200 the right choice for modular devices that use LVDS as internal physical layer.

The next ASIC, the ETI100 with additional EtherCAT ports, even more memory and parallel  $\mu$ C interface is in production and is expected back for testing at the end of January 07. Since it comes in BGA128 housing (10x10 mm) the "big" ASIC in fact is small, too.

→ ETG booth at SPS/IPC/DRIVES: Hall 6, Booth 309

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